SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

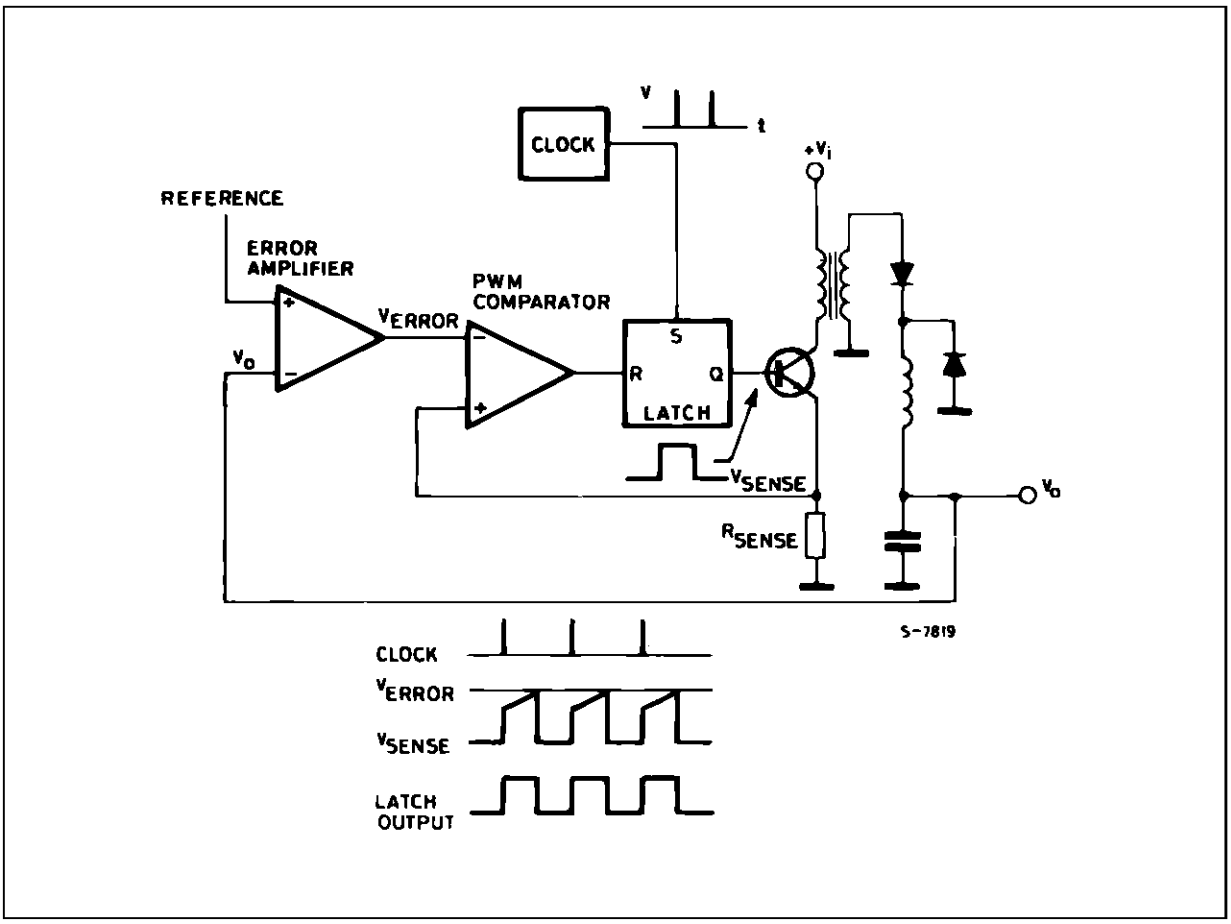
The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives : good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Figure 1 : Two-loop Current-mode Control System.



Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved ; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single pole (filter capacitor in parallel with load) response.

One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler and better behaved, as illustrated in figure 3. Capacitor C_i and resistor R_{iz} in figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output vol-tage. The recovery time is R_{iz} C_i, which may be milleseconds. However, the compensation network of figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Figure 2 : Inductor Looks Like a Current Source to Small Signals.

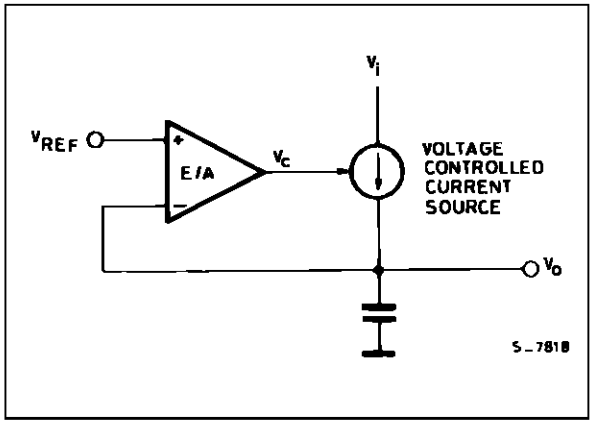


Figure 3 : Required Error Amplifier Compensation for Continuous Inductor Current Designs using (a) Duty-cycle Control and (b) Current-mode Control.

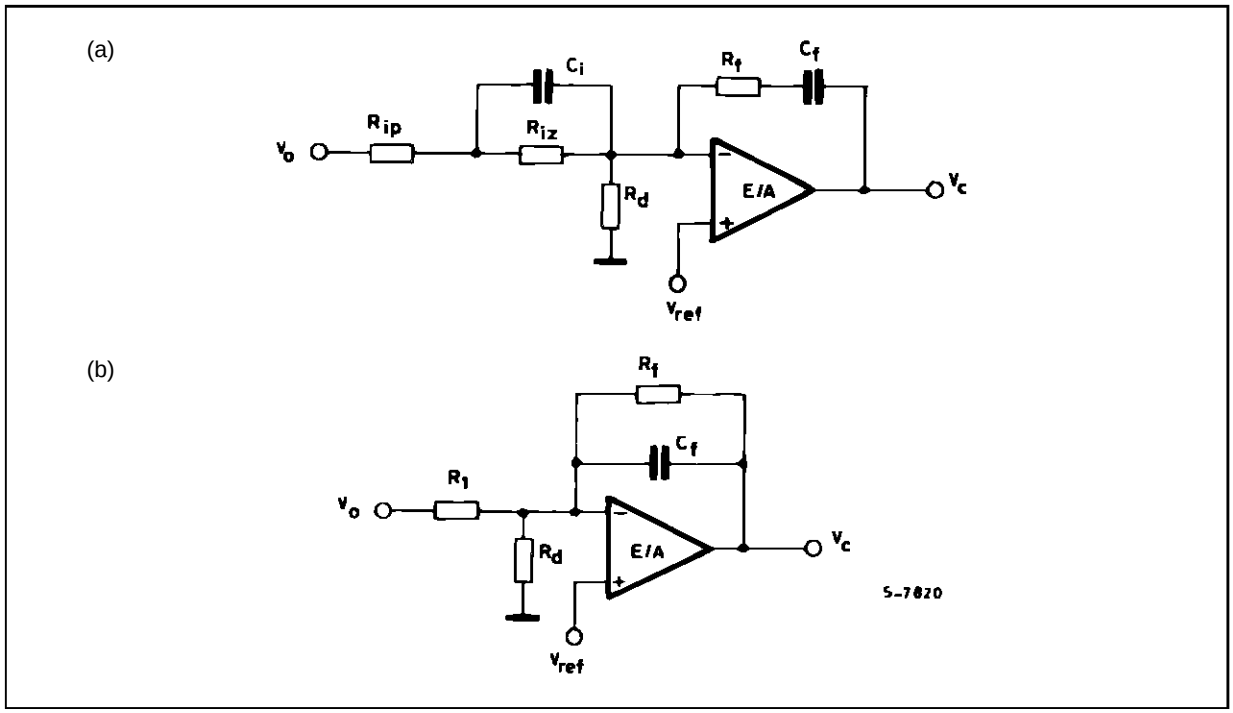
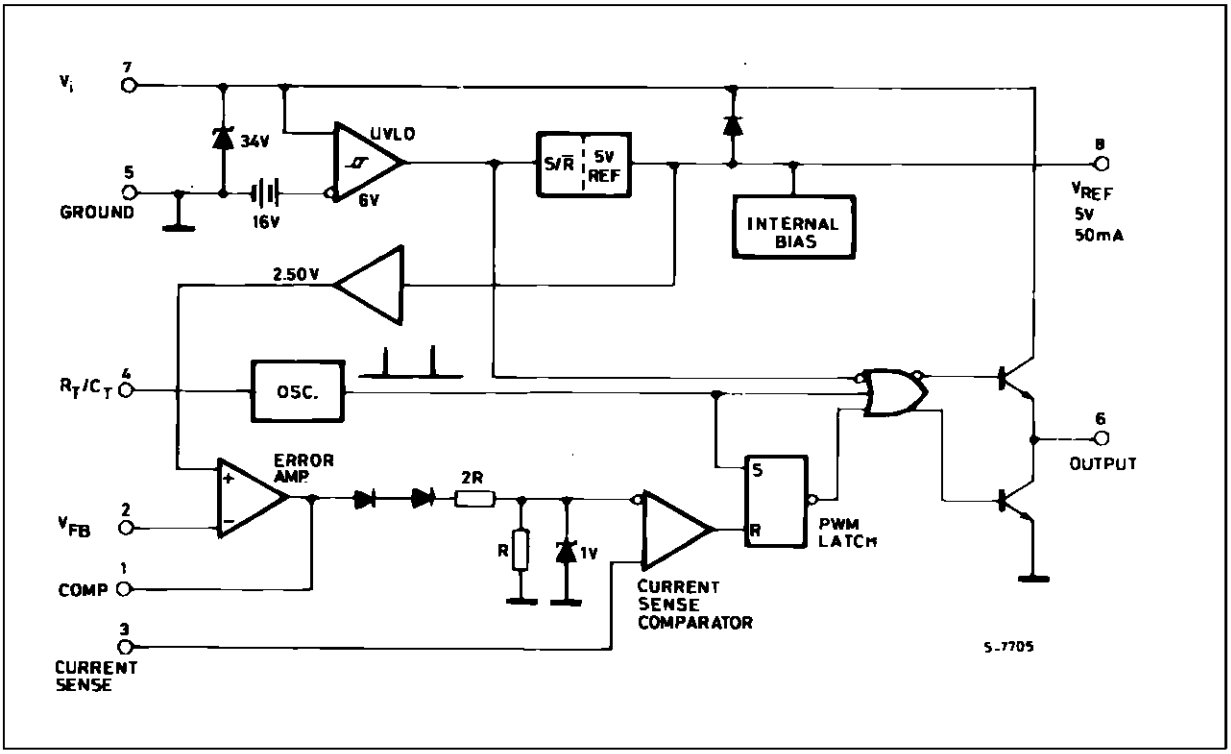


Figure 4 : UC3842 Block Diagram.



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in figure 4. This IC will operate from a low impedance DC source of 10 V to 30 V. Operation between 10 V and 16 V requires a start-up bootstrap to a voltage greater than 16 V in order to overcome the undervoltage lockout. V_{CC} is internally clamped to 34 V for operation from higher voltage current-limited sources ($I_{CC} \leq 30$ mA).

UNDER-VOLTAGE LOCKOUT (UVLO)

This circuit insures that V_{CC} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16 V and 10 V respectively. The 6 V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16 V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90 V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130 V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10 μA), if not shunted to ground, could pull high the gate of a POWERMOS. A 100 kΩ shunt, as showing in figure 6, will hold the gate voltage below 1V.

Figure 5 : (a) Under-voltage Lockout and (b) Supply Current Requirements.

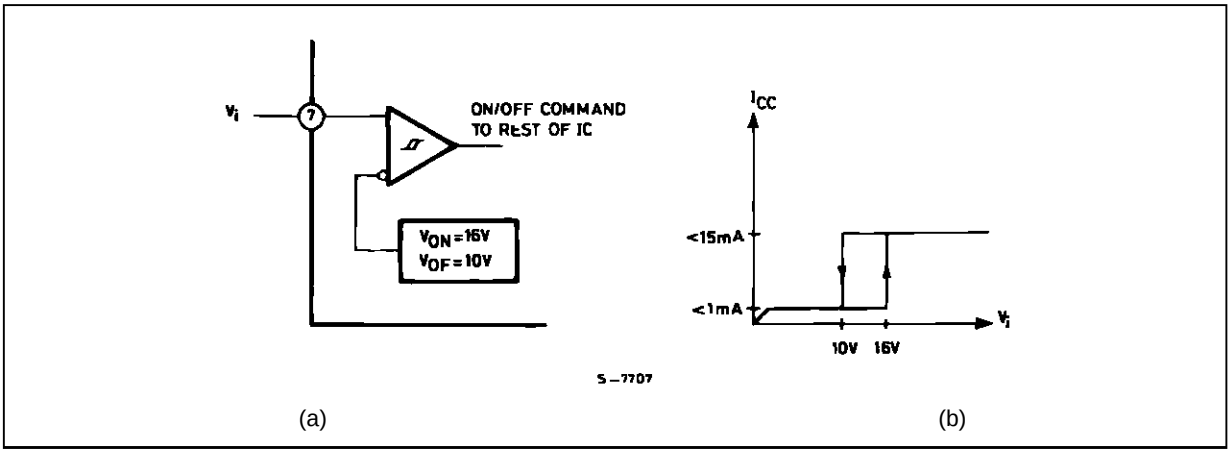
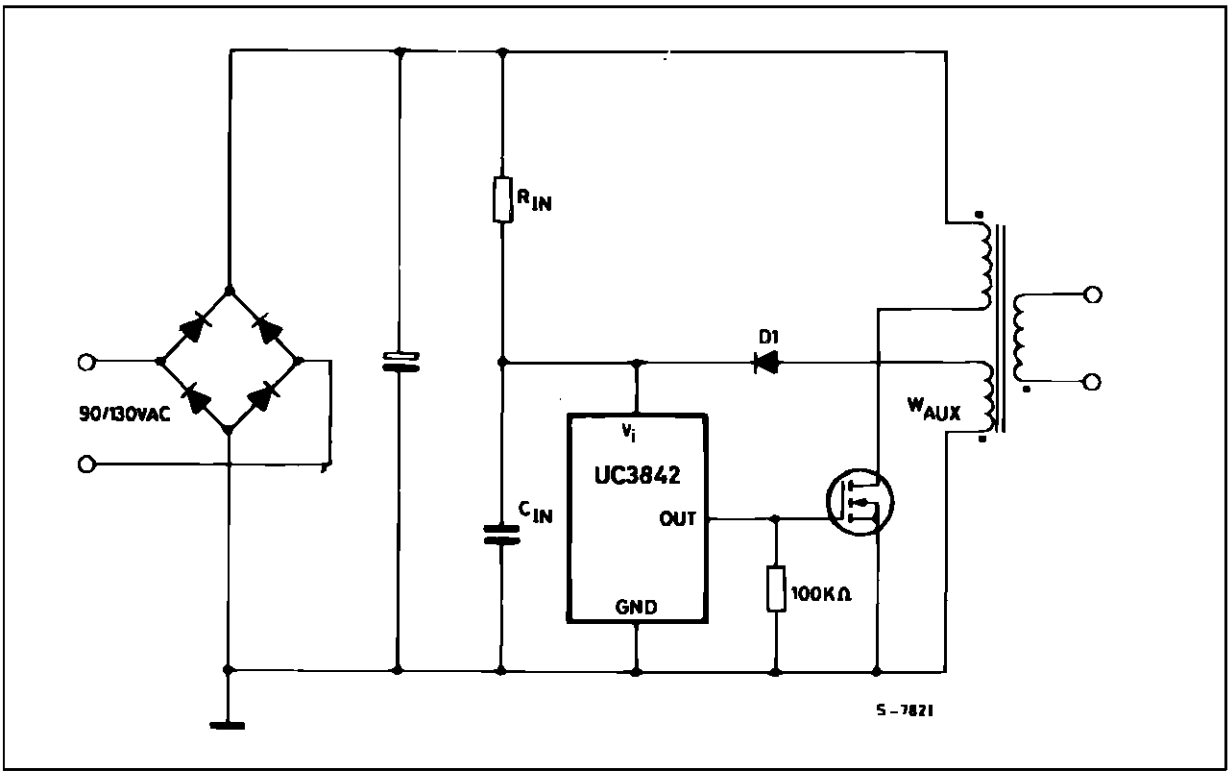


Figure 6 : Providing Power to the UC3842.



OSCILLATOR

The UC3842 oscillator is programmed as shown in figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5 V) through R_T, and discharged by an internal current source. Charge and discharge times are given by :

$$t_c \approx 0.55\, R_T\, C_T$$

$$t_d \approx R_T\, C_T \ln\left(\frac{0.0063\, R_T - 2.7}{0.0063\, R_T - 4.0}\right)$$

frequency, then, is : $f = \frac{1}{t_c + t_d}$

For $R_T > 5\ k\Omega$, t_d is small compared to t_c, and :

$$f \approx \frac{1}{0.55\, R_T\, C_T} \approx \frac{1.8}{R_T\, C_T}$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to :

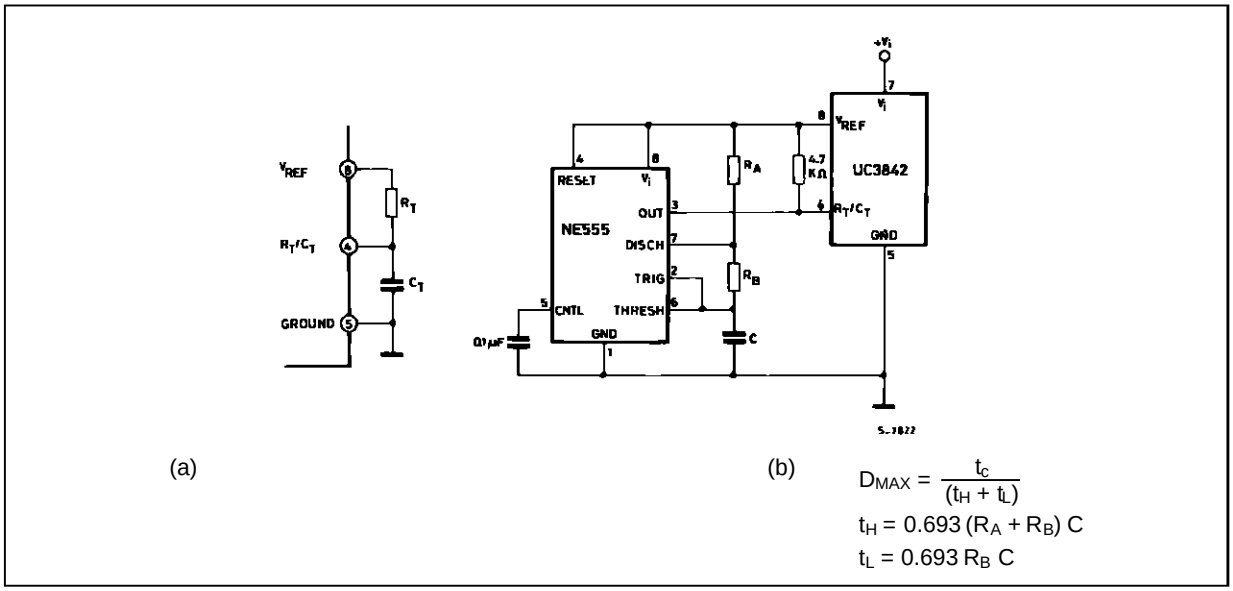
$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{\tau}$$

where $\tau = 1/f$ = switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over temperature and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be ~ 20 % less than the clock frequency.

Figure 7 : (a) Oscillator Timing Connections and (b) Circuit for Limiting Duty Cycle.



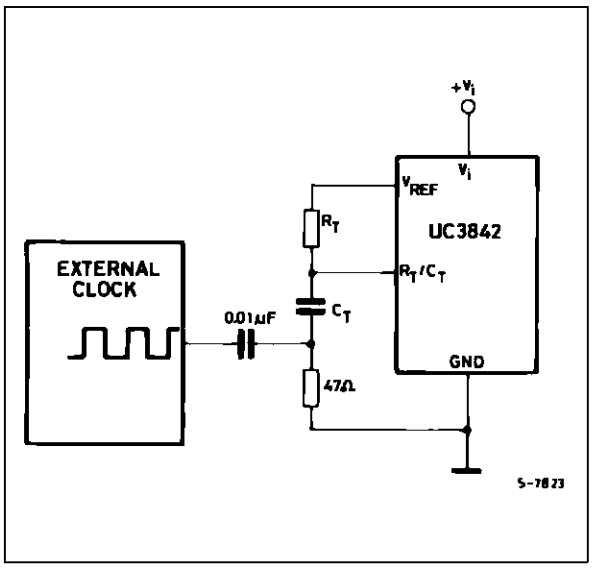
(a) (b)

$$D_{MAX} = \frac{t_c}{(t_H + t_L)}$$

$t_H = 0.693\,(R_A + R_B)\,C$

$t_L = 0.693\,R_B\,C$

Figure 8 : Synchronization to an External Clock.



ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in figure 9. The non-inverting input is not brought out to a pin, but is internally biased to 2.5 V ± 2 %. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\ \pi R_f C_f$. R_f and C_f are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_i and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0dB) at $f \approx f_{switching}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of figure 10b provide this pole.

The E/A output will source 0.5 mA and sink 2 mA. A lower limit for R_f is given by :

$$R_{f\,(MIN)} \approx \frac{V_{E/A\ OUT(max)} - 2.5\ V}{0.5\ mA} = \frac{6\ V - 2.5\ V}{0.5\ mA} = 7\ k\Omega$$

E/A input bias current (2 µA max) flows through R_i, resulting in a DC error in output voltage (V_o) given by :

$$\Delta\ V_{o(max)} = (2\ \mu A)\ R_i$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~ 10 MHz and above.

Figure 9 : UC3842 Error Amplifier.

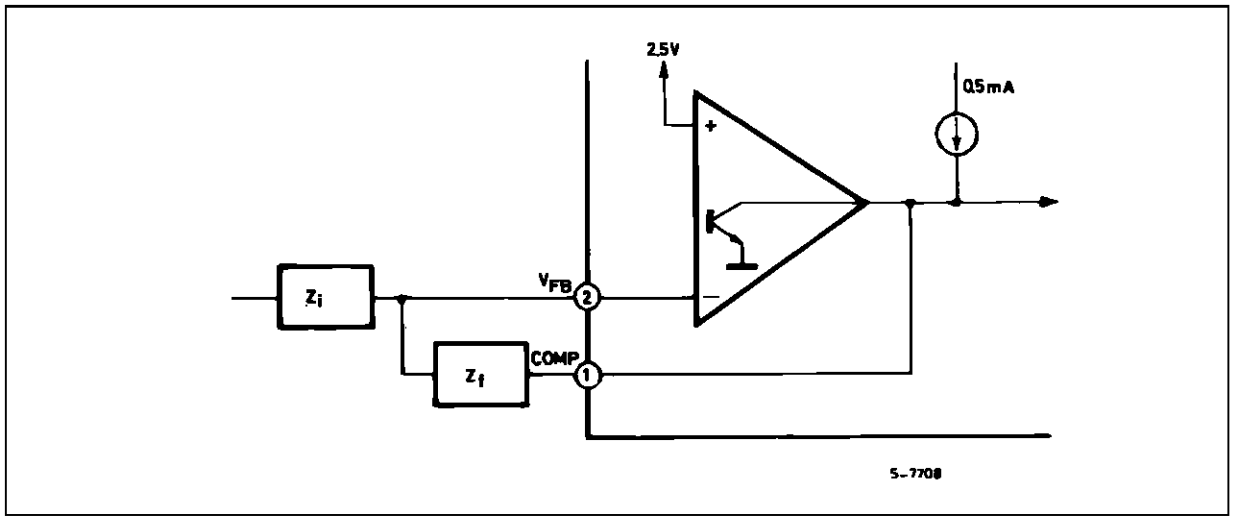


Figure 10 : (a) Error Amplifier Compensation Addition Pole and (b) Needed for Continu ous Inductor-current Boost ad Flyback.

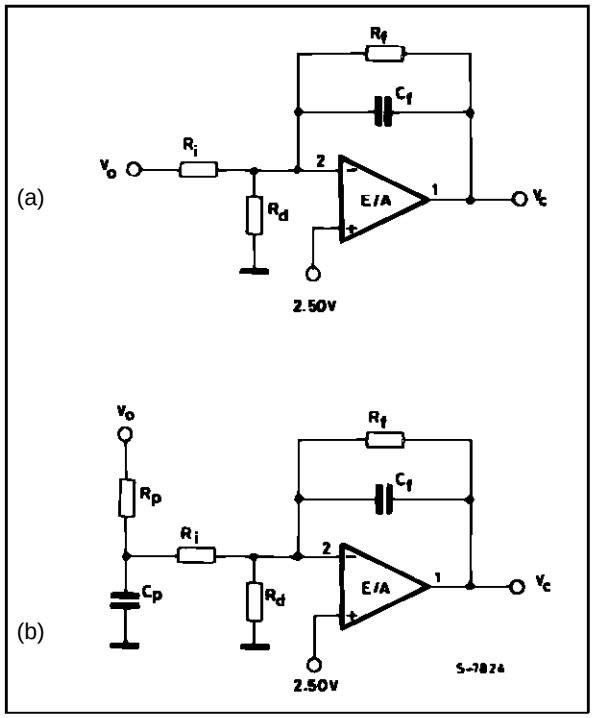
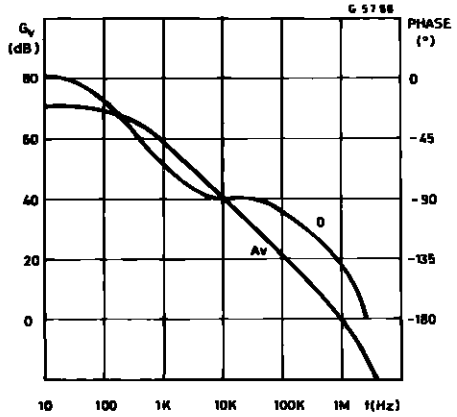


Figure 11 : Error Amplifier Open-loop Frequency Response.



CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation :

$$V_{RS}\,(pk) = \frac{V_C - 1.4\ V}{3}$$

where : V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-reference sensing. The relation between V_C and peak current in the power stage is given by :

$$i_{(pk)} = N\left(\frac{V_{RS}(pk)}{R_S}\right) = \frac{N}{3\,R_S}\,(V_C - 1.4)$$

where : N = current sense transformer turns ratio.
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is :

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in figure 13, current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or interwinding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1 V (figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by :

$$i_{MAX} = \frac{N \cdot 1\ V}{R_S}$$

Figure 12 : Current Sensing.

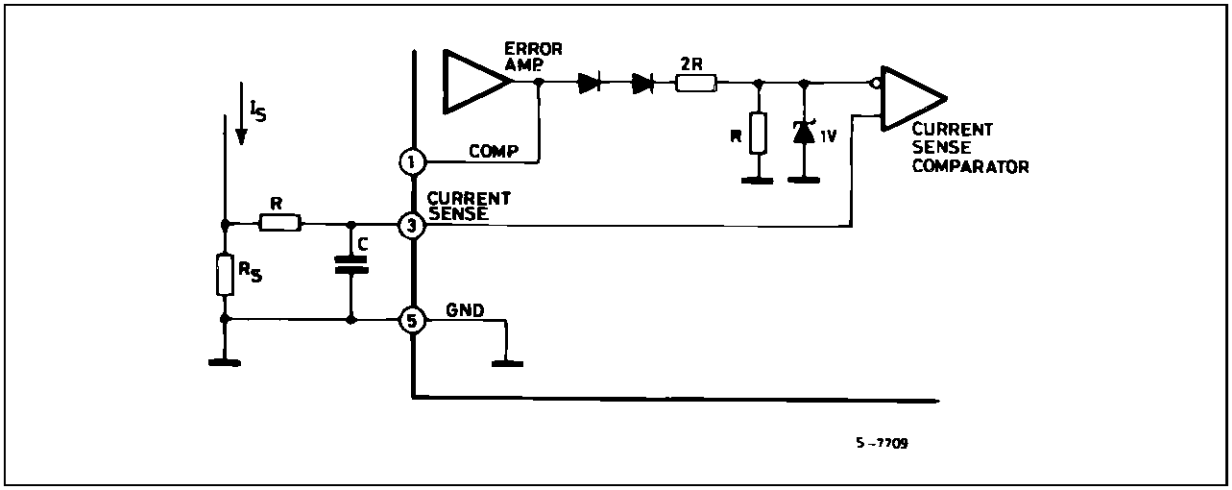
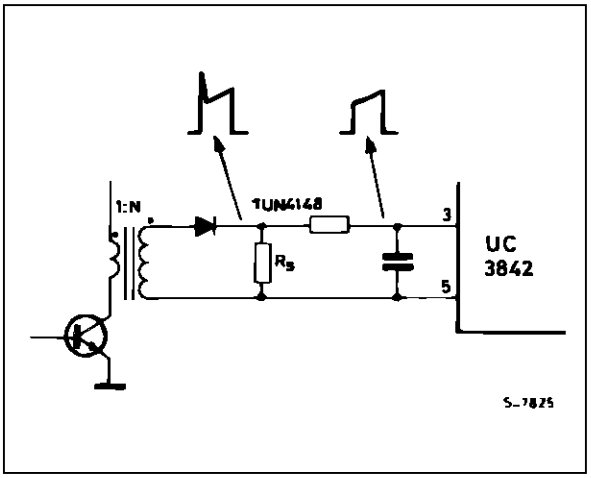


Figure 13 : Transformer-coupled Current Sensing.



TOTEM-POLE OUTPUT

The UC3842 has a single totem-pole output. The output transistors can be operated to ± 1 A peak current and ± 200 mA average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a power MOS gate.

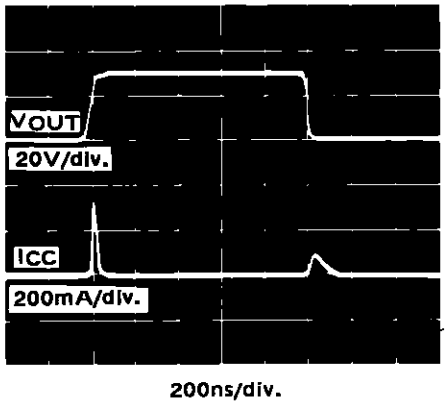
Cross-conduction between the output transistors is minimal, as figure 14 shows. The average added power due to cross-conduction with V_i = 30 V is only 80 mW at 200 kHz.

Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple circuit of figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents (10 µA maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be levelshifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

PWM LATCH

This flip-flop, shown in figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Figure 14 : Output Cross-conduction.



SHUTDOWN TECHNIQUES

Shutdown of the UC3842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below 1 V. Either method causes the output of the PWM comparator to be high (refer to block diagram, figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10 V). At this point all internal bias is removed, allowing the SCR to reset.

Figure 15 : Direct POWERMOS Drive.

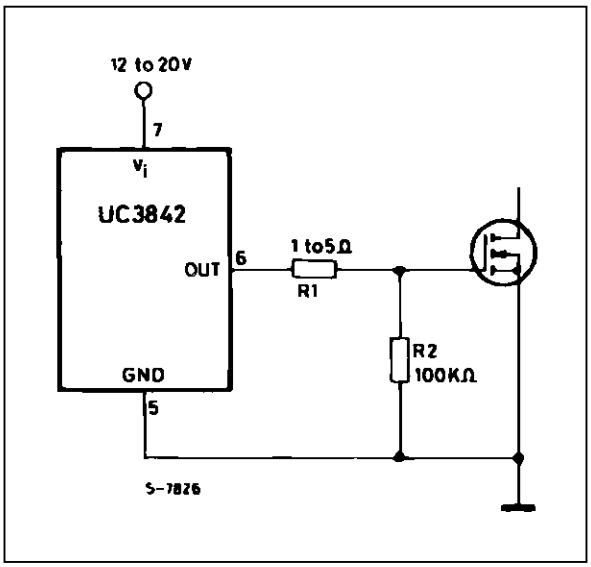


Figure 16 : Isolated POWERMOS Drive.

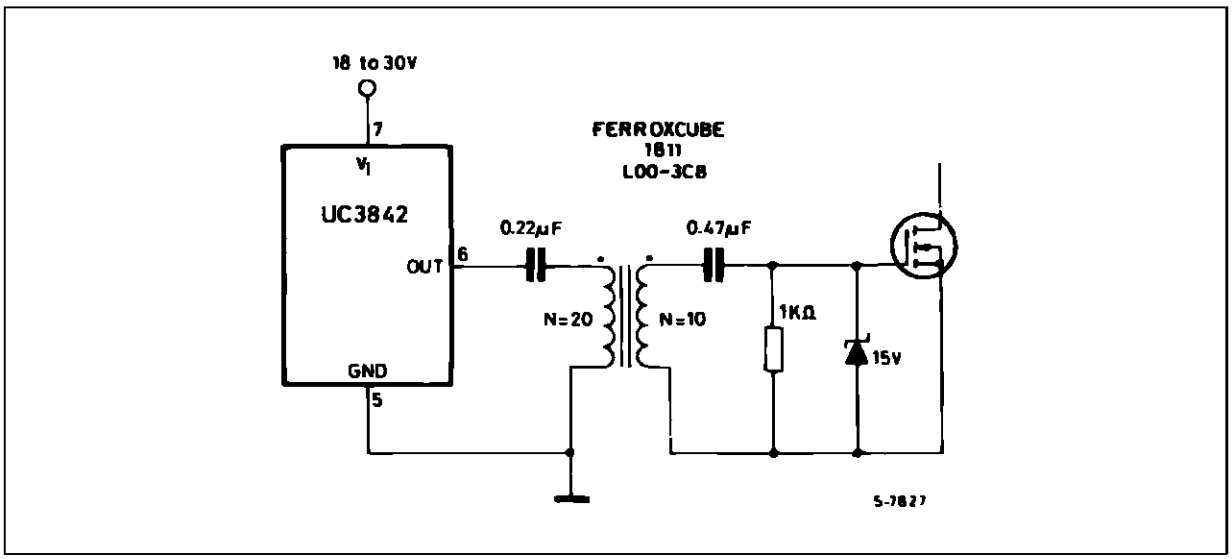
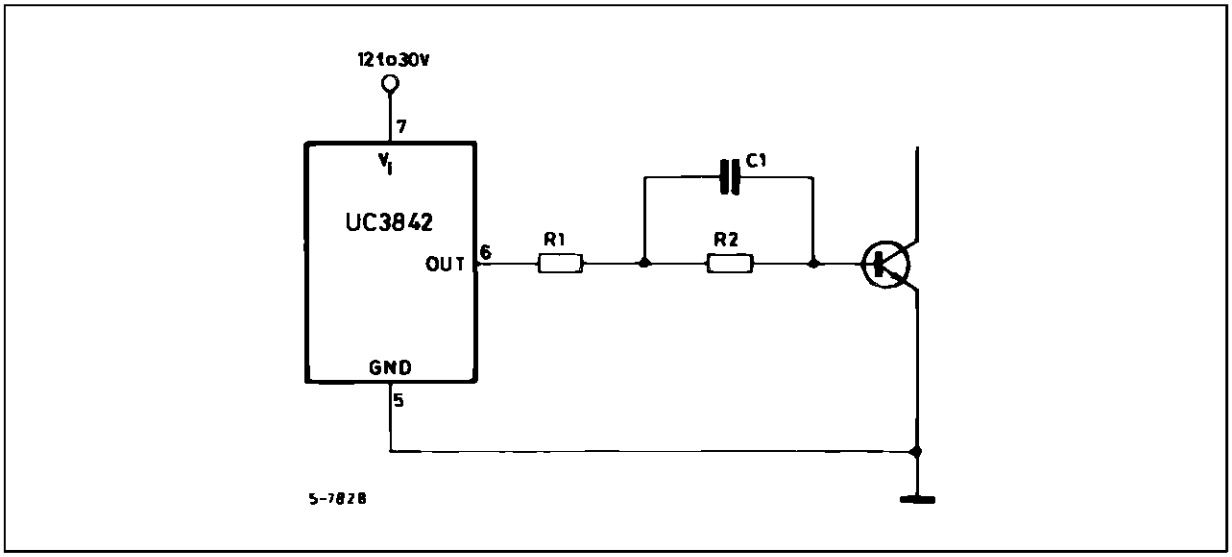


Figure 17 : Bipolar Drive with Negative Turn-off Bias.



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

SLOPE COMPENSATION PREVENTS INSTABILITIES

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations when operated at duty cycles greater than 50 %.

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 18 : Shutdown Achieved by
(a) Pulling Pin 3 High
(b) Pulling Pin 1 Low.

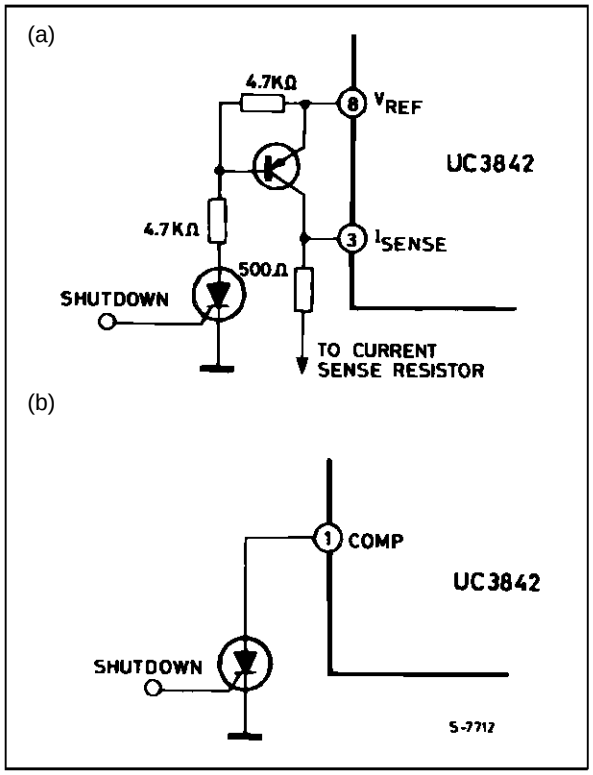


Figure 19 illustrates the slope compensation technique. In figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_o) and inductance (L) :

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_o}{L} = \frac{-(V_F + V_o)}{L}$$

where : V_F = forward voltage drop across the freewheeling diode. The actual slope (m_2) of the dashed lines in figure 19a is given by :

$$m_2 = \frac{R_S}{N} \cdot \frac{di_L}{dt} = \frac{-R_S (V_F + V_o)}{NL}$$

where : R_S and N are defined as the "Current Sensing" section of this paper.

In figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and practice is most easily derived from the control chip oscillator as shown in figure 20a. The sawtooth slope in figure 19b is $m = m_2/2$. This particular slope value is significant in that it yields "perfect" current-mode control ; i.e. with $m_2/2$ the average inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50 % duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_{V(E/A)}$) at half the switching frequency ($f_s/2$) is kept below a threshold value (reference 6) :

$$A_{V\,(E/A)} \Big|_{\substack{m = m2 \\ f = f_s/2}} < \frac{\pi\, 2\, C_O}{4\, \tau}$$

where : C_o = sum of filter and load capacitance
$\tau = 1/f_s$

Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required ; for very noisy circuits the optimum amount of slope compensation is best found empirically.

Once the required slope is determined, the value of R_{SLOPE} in figure 20a can be calculated :

$$3\ m = \frac{\Delta V_{RAMP}}{\Delta\, t_{RAMP}} \cdot A_{V(E/A)} = \frac{0.7\ V}{\tau/2} \left(\frac{R_{SLOPE}}{Z_F \mid f_s} \right) = \frac{1.4}{\tau} \left(\frac{R_{SLOPE}}{Z_F \mid fs} \right)$$

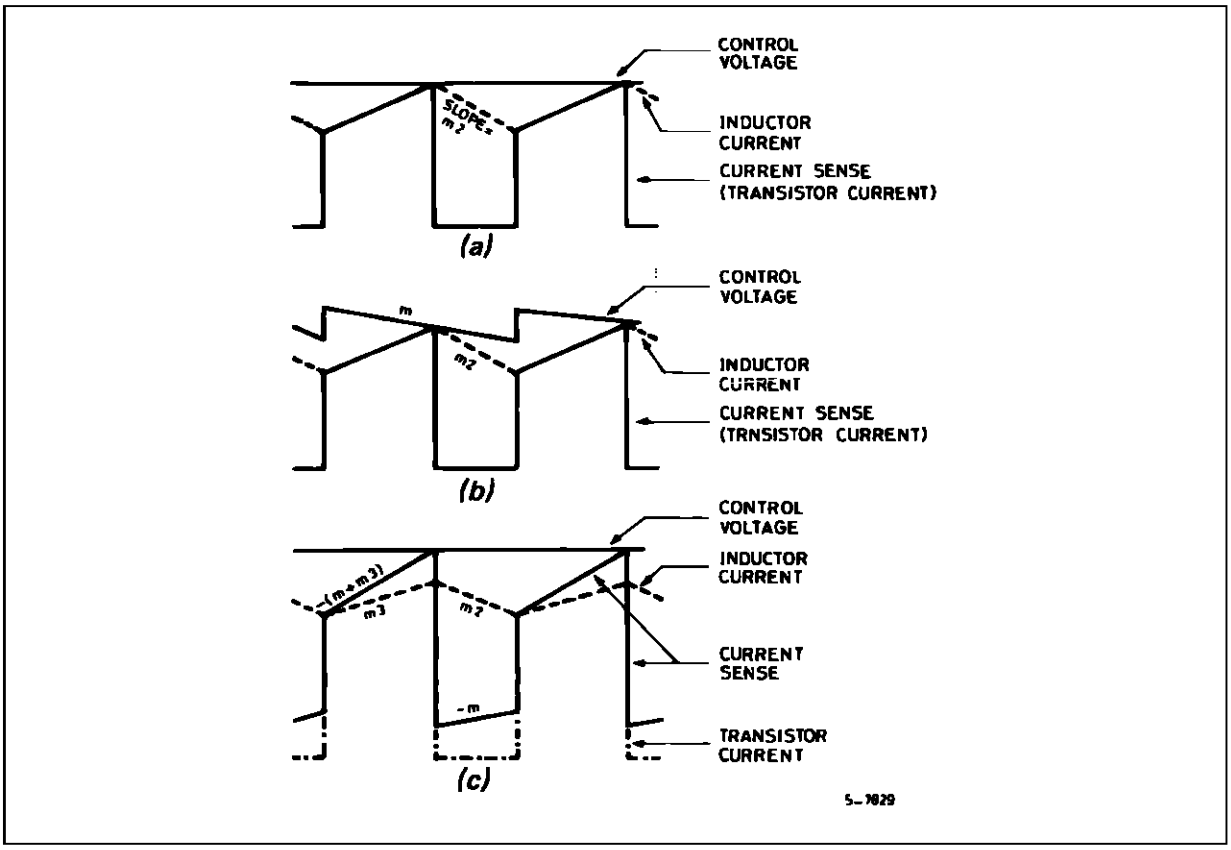
$$R_{SLOPE} = \frac{3\, m\, \tau}{1.4}\ (Z_F \mid f_s) = 2.1 \cdot m \cdot \tau \cdot Z_F \mid f_s$$

where : $Z_F \mid f_s$ is the E/A feedback impedance at the switching frequency.

For $m = m_L$: $\Delta\tau_{RAMP}$

$$R_{SLOPE} = 1.7\, \tau \left(\frac{R_s\, (V_F + V_O)}{NL} \right) Z_F \mid f_s$$

Figure 19 : Slope Compensation Waveforms :
(a) No Comp.
(b) Comp. Added to Control Voltage.
(c) Comp. Added to Current Sense.



Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least 3 f_s.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now :

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \left(\frac{R_f}{R_f + R_{SLOPE}} \right) = \frac{0.7}{\tau/2} \left(\frac{R_f}{R_f + R_{SLOPE}} \right)$$

$$R_{SLOPE} = \frac{1.4\, R_f}{m\tau} - R_f = R_f \left(\frac{1.4}{m\tau} - 1 \right)$$

For $m = m_2$:

$$R_{SLOPE} = R_f \left(\frac{1.4\, NL}{R_S\, (V_F + V_O)\, \tau} - 1 \right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} >> R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \leq 5\, R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in figure 21.

Figure 20 : Slope Compensation Added (a) to Control Signal or (b) to Current Sense Waveform.

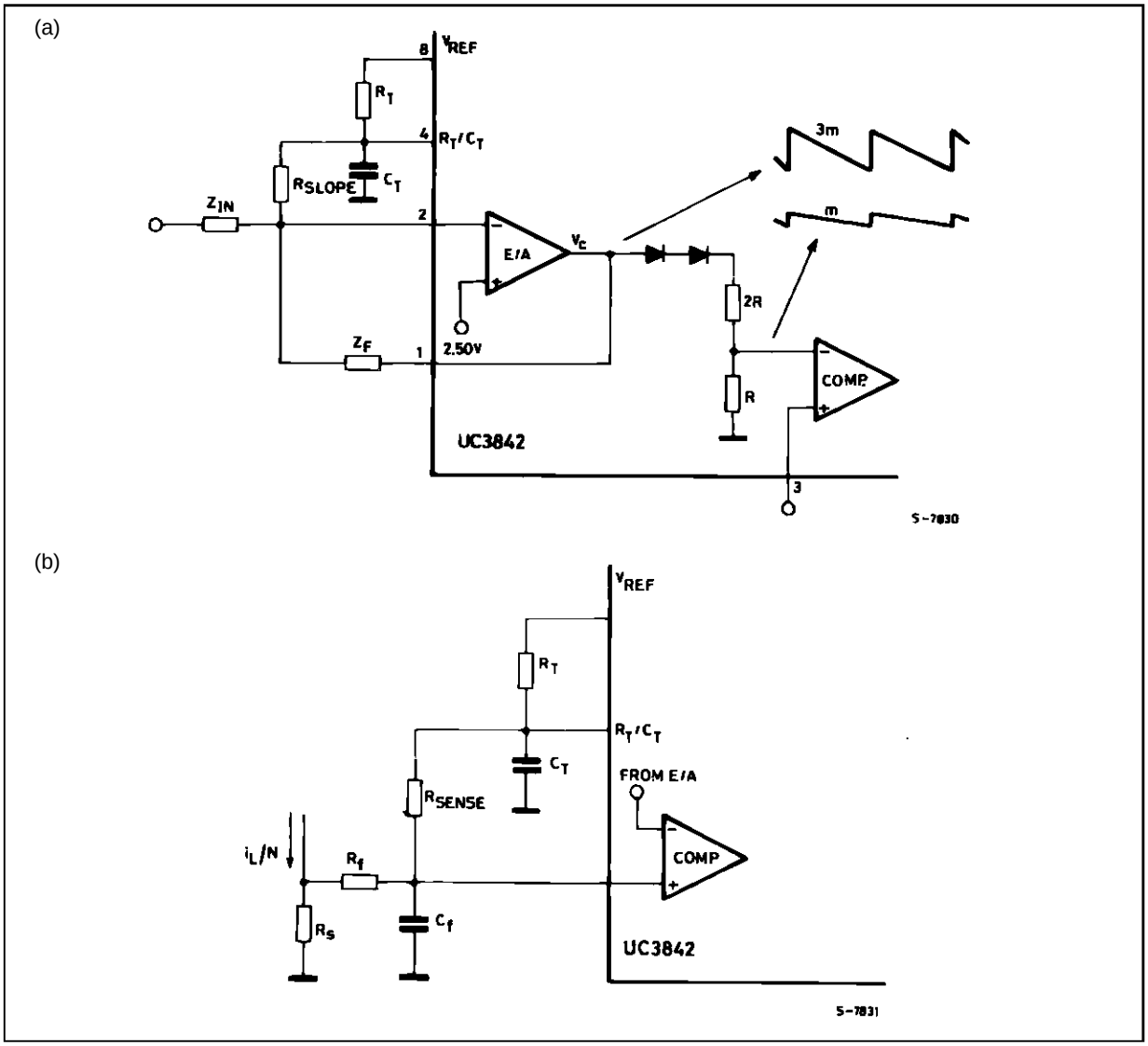
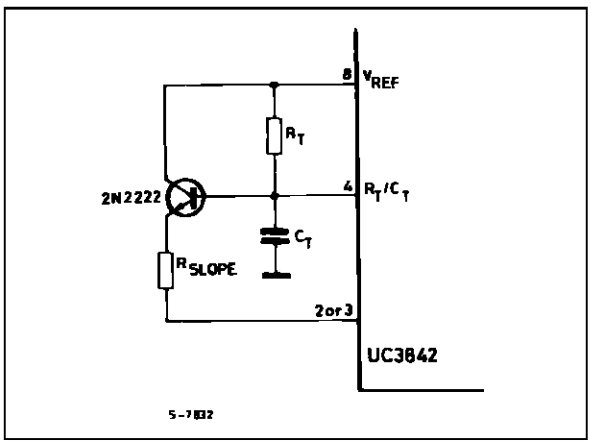


Figure 21 : Emitter-follower Minimizes Load at R_T/C_T Terminal.



NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedance decrease at critical points in a circuit.

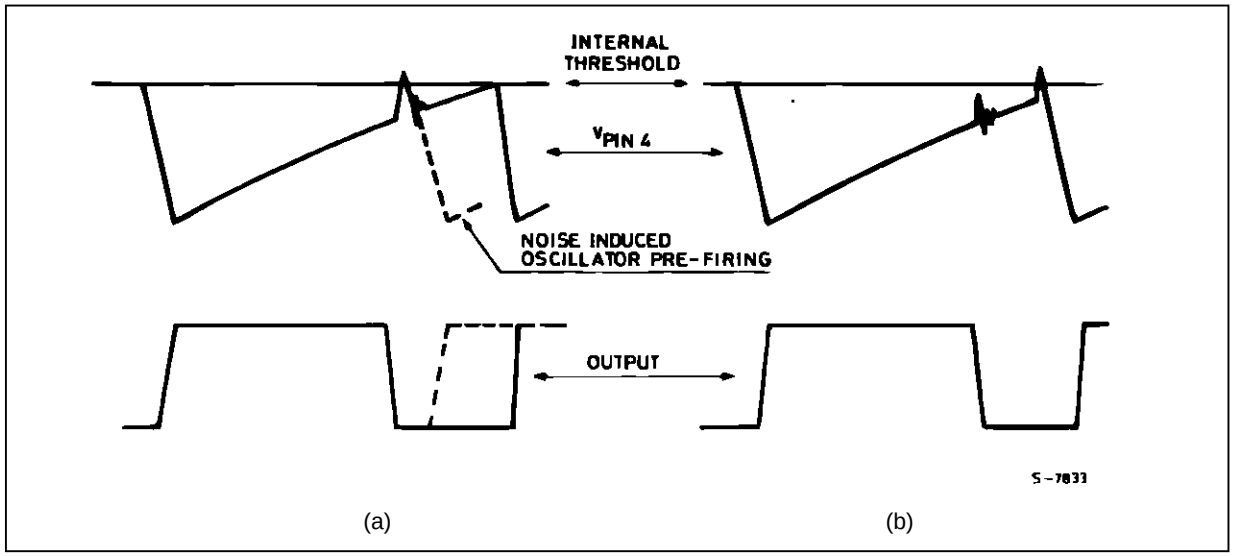
One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise.

Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic bypass capacitors (0.1 µF) from V_I and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~ 2.7 V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~ 1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving POWERMOS. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of figure 8 results in an R_T/C_T waveform like that of figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

Figure 22 : (a) Noise on Pin 4 Can Cause Oscillator to Pre-trigger.
(b) With External Sync. Noise Does not Approach threshold Level.

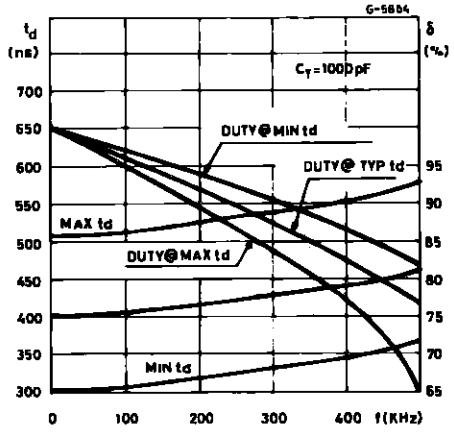


MAXIMUM OPERATING FREQUENCY

Since output deadtime varies directly with C_T, the restraint on minimum C_T (1000 pF) mentioned above results in a minimum deadtime varies for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in figure 23. Above 100 kHz, the deadtime significantly reduces the maximum duty cycle obtainable at the UC3842 output (also show in figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as 500 kHz. Operation at higher frequencies is not recommended because the deadtime become less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400 ns represents 10 % of the switching period at 250 kHz and 20 % at 500 kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~ 250 kHz, may of the advantages of higher-frequency operation are lost.

Figure 23 : Deadtime and Maximum Obtainable Duty-cycle vs. Frequency with Minimum Recommended C_T.



CIRCUIT EXAMPLES

1. OFF-LINE FLYBACK

Figure 24 shows a 25 W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS :

Line Isolation : 3750 V

Switching Frequency : 40 kHz

Efficiency @ full load : 70 %

Input Voltage 95 VAC to 130 VAC (50Hz/60Hz)

Output Voltage :

A. + 5 V, 5 % : 1 A to 4 A load
Ripple voltage : 50 mV P-P Max.

B. + 12 V, 3 % : 0.1 A to 0.3 A load
Ripple voltage : 100 mV P-P Max

C. – 12 V, 3 % 0.1 A to 0.3 A load
Ripple voltage : 100 mV P-P Max

Figure 24 : 25W off-line Flyback Regulator.